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May 6, 2005

Mail Stop Amendment
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re:	Applicant(s):	Harari et al.		
	Title:	Flash EEProm System		
	Application No.:	09/759,119	Filing Date:	January 11, 2001
	Examiner:	Tan, Nguyen	Group Art Unit:	2827
	Docket No.:	SNDK.A06US5	Conf. No.:	1201

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

(1) Return Receipt Postcard;
(2) This Transmittal Letter (1 page in duplicate);
(3) Supplemental Information Disclosure Statement (2 pages);
(4) PTO Form 1449 (5 pages) and

☐ No additional fee is required.

☒ Fee for Information Disclosure Statement

☒ Please charge any additional fees required and credit any overpayment to our Deposit Account No. 502664.

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 6, 2005.

Ann-Ellice Parker

Ann-Ellice Parker

Respectfully submitted,

Gerald P. Parsons
Reg. No.: 24,486

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Harari et al.		
Title:	Flash EEProm System		
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Ann-Ellice Parker

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INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) call(s) the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application.

☒ Copies of the documents listed on the accompanying Form PTO-1449 that are not enclosed were previously submitted in Applications No. 09/188,417, filed November 9,1998, 08/771,708 filed December 20, 1996, 08/174,768 filed December 29, 1993, 07/963,838 filed October 20, 1992, and 07/337,566 filed April 13, 1989 from which this Application claims an earlier effective filing date.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a

(3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(c). A check including $180.00 for the information disclosure statement fee under 37 C.F.R. § 1.17(p), is enclosed. The Commissioner is authorized, however, to charge any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664.

Respectfully submitted,

Gerald P. Parsons
Reg. No. 24, 486

May 5, 2005
Date

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U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.A06US5	09/759,119
	Applicant(s)	**Conf. No.**
(Use several sheets if necessary)	Harari et al.	1201
(Form PTO-1449)	**Filing Date**	**Group**
	January 11, 2001	2827

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	1	4,090,258	5/16/78	Cricchi			
	2	4,149,270	4/10/79	Cricchi et al.			
	3	4,181,980	1/1/80	McCoy			
	4	4,253,059	2/24/81	Bell et al.			
	5	4,272,830	6/9/81	Moench			
	6	4,279,024	7/14/81	Schenk			
	7	4,393,475	9/1/81	Stark			
	8	4,393,475	7/12/83	Kitagawa et al.			
	9	4,415,992	11/15/83	Adlhoch			
	10	4,460,982	7/17/84	Gee et al.			
	11	4,475,194	10/2/84	La Valee et al.			
	12	4,495,602	1/22/85	Sheppard			

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	13	GB2061651	1981	United Kingdom				
	14	GB2029145	1980	United Kingdom				
	15	JP6225769	1988	Japan			X	
	16	JP5931158	1984	Japan				X
	17	DE363782	1987	Germany			Abstract	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	18	Bleiker et al., "A Four State EEPROM Using Floating-Gate Memory Cells", IEEE Journal of Solid-State Circuits, Vol. Sc-22. No. 3, June 1987, pp.460-463.
	19	Torelli et al., "An Improved Method for Programming A Word Erasable EEPROM", Alta Frequenza, Vol. 52, Nov.- Dec. 1983, No. 6, pp. 487-494.
	20	Stark, "Two Bits Per Cell ROM", Digest of Papers Spring COMCONS 81, Feb. 23-26, VLSI LABORATORY, pp. 209-212.

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	21	4,586,163	4/29/86	Koike			
	22	4,612,629	9/16/86	Harari			
	23	4,677,590	6/30/87	Arakawa			
	24	4,718,041	1/5/88	Baglee et al.			
	25	4,733,394	3/22/88	Giebel			
	26	4,752,929	6/21/88	Kantz			
	27	4,779,272	10/18/88	Kohda et al.			
	28	4,799,195	1/17/89	Iwahashi et al.			
	29	4,807,188	2/21/89	Casagrande			
	30	4,890,231	2/28/89	Shannon et al.			
	31	4,811,294	3/7/89	Kobayashi et al.			

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	32	DE3831538	1989	Germany			Abstract	
	33	JP62-188100	1987	Japan			X	
	34	JP0123878	1989	Japan				
	35	JP0146949	1989	Japan				

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	36	Furuyama et al., "An Experimental 2-BIT/CELL Storage Dram for Macro Cell or Memory-on-Logic Application", IEEE Custom Integrated Circuits Conference, May 1988, pp. 4.4.1-4.4.4.
	37	Krick, "Three-State MNOS FET Memory Array", IBM Technical Disclosure Bulletin, Vol. 18, No.12, May 1976, pp. 4192-4193.
	38	Alberts et al., "Multi-Bit Storage Fet Earom Cell", IBM Technical Disclosure Bulletin, Vol. 24, No.7A, Dec. 1981, pp. 3311-3314, 4193.

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	38	4,847,808	7/11/89	Kobatake			
	39	4,870,618	9/26/89	Iwashita			
	40	4,943,962	7/24/90	Imamiya et al.			
	41	4,956,816	7/24/90	Atsumi et al.			
	42	4,980,861	12/25/90	Herdt et al.			
	43	4,999,813	3/12/91	Ohtsuka et al.			
	44	5,003,510	3/26/91	Kamisaki			
	45	5,053,990	10/1/91	Kriefels et al.			
	46	5,095,344	3/10/92	Harari			
	47	5,136,021	11/10/92	Mehrota et al.			
	48	5,297,148	3/22/94	Harari et al.			
	49	5,357,462	10/18/94	Tanaka et al.			

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	50	Horiguchi et al. "An Experimental Large-Capacity Semiconductor File Memory Using 16-LEVEL/CELL storage", IEEE Journal of Solid-State Circuits, Vol. 23, Feb.1998, No.1, pp. 27-33.
	51	Masuoka et al. "A 256-KBIT Falsh EEPROM Using Triple-Polysilicon Technology", IEEE Journal of Solid-State Circuits, Vol. SC-22, No.4, pp.548-552, New York, USA, August 1987.
	52	Berenga et al. "E2-PROM TV Synthesizer", 1978 IEEE International Solid-State Circuits Conference: ISCCC 78", February 17, 1978, pp.196-197.
	53	Kynett et al. "An In-System Reprogrammable 32K X 8 CMOS Flash Memory", IEEE Journal of Solid-State-Circuits, Vol. 23, No.5, Log Number 8822443, October 1988, pp. 1157-1163.
	54	Klingman, "Microprocessor Systems Design", Prentice-Hall, Inc. pp.30-31, 1977.
	55	SGS-ATES "Excerpts From a 1983 Data Book", SGS-Ates Group, 45 pp., Nov. 1983.
	56	Torelli et al., "Non-Volatile Station Memory and Remote-Control Receiver and Memory Display Driver", IEEE Transactions on Consumer Electronics, Vol. CE-29, No.3, pp.103-13, August 1983.
	57	Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver in a Single Chip", IEEE Digest of Technical Papers, CAT. No.: 83CH1872-1, 2 pp., June 8, 1983

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	58	5,361,227	1/1/94	Tanaka et al.			
	59	5,602,987	2/11/97	Harari et al.			
	60	4,959,812	9/25/90	Momodomi et al.			
	61	4,939,690	7/3/90	Momodomi et al.			
	62	4,996,669	2/26/91	Endoh et al.			
	63	5,163,021	1992	Mehrotra et al.			
	64	5,172,338	1992	Mehrotra et al (Reexamination)			
	65	5,657,270	1997	Ohuchi et al.			
	66	5,793,696	8/11/98	Tanaka et al.			
	67	5,831,903	11/03/98	Ohuchi et al.			

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	68	Caironi et al., "A TV Frequency Synthesis System With a Single Chip Microprocessor Interface Including Non-Volatile Memory", IEEE Transactions on Consumer Electronics", Vol. CE-28, No.3, pp.363-71, August 1982.
	69	Torelli, "An LSI Technology Fully Compatible EAROM Cell", Component Elettronic SpA, No. 6, Vol. LI, 7 pp. 1982.
	70	Torelli et al., PLL2K-PLL Frequency Synthesizer for 30 Programs", SGS-ATES, Technical Note #152, pp.1-16, 1982.
	71	Torelli et al. "Single Chip, 16 Station TV Digital Tuning System", SGS Technical Note #170, pp.1-19, 1984.
	72	Scrocchi et al. "EPM32-Electronic Program Memory System for TV (32 stations)" SGS-ATES, Technical Note#153, pp. 1-19, 1982.
	73	SGS-ATES. "PLL TV Microcomputer interface", SGA-ATES, MOS Integrated Circuits/M206, 15 pp. June 1982.

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	76	Gee et al., "An Enhanced 16K E2PROM", IEEE Journal of Solid-State Circuits, Vol. SC-17, No.5, October 1982, pp. 828-832.
	77	Kynett et al., "A 90-ns One Million Erase/Program Cycle 1-Mbit Flash Memory", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, October 1989, pp. 1259-1263.
	78	Tanaka et al., "A 4-Mbit NAND-EEPROM with Tight Programmed Vt Distribution", 1990 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 105-106.
	79	IBM Technical Disclosure Bulletin "EPROMgramming Device", Vol. 29, No.9, February 1987, pp. 4145-4146.
	80	"Bipolar /MOS Memories Data Book", Advanced Micro Devices, ISSN 0888-4714, pp.6-1-6-14, 1986
	81	SEEQ Data Book 1988/89 SEEQ Technology, Inc. pp.3-1-3-7

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